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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,372	07/31/2001	Vadim Gutnik	5347-205	2525

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EXAMINER	
CHUNG, PHUNG M	
ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
10/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/919,372	GUTNIK ET AL.	
	Examiner	Art Unit	
	PHUNG My CHUNG	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date. _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 1-13 and 19-24 is withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-4, 6-10 and 12-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, III (5,146,585).

As per claim 1, Smith, III, discloses a clock distribution circuit, comprising:

A first clock circuit (TOD source 12a of Figs. 1 and 2) that is configured to generate a first clock signal responsive to an error signal;

A second clock circuit (TOD source 12b of Fig. 1) that is configured to generate a second clock signal responsive to the error signal; and

A phase detector circuit (phase comparator 38 of Fig. 2) that connects the first clock circuit (TOB 12a through phase adjuster 36) to the second clock circuit (TOD 12b, Fig. 2 through line 52 of Fig. 1) and is configured to generate the error signal (56) responsive to the first and the second clock signals. (See Figs. 1-2, col. 2, lines 65-67 to col. 3, lines 1-5 and lines 23-67 to col. 4, lines 1-60, and col. 12, claims 9-10). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the first clock circuit (TOD source 12a of Fig. 2) into the second clock circuit (TOD source 12b of Fig. 1) or vice versa so that the phase detector circuit (phase comparator 38) can be configured to generate the error signal responsive to the first and the second clock signals.

As per claim 2, the teaching of Smith, III has been discussed above. Smith, III does not disclose a third clock circuit that is configured to generate a third clock signal responsive to a second error signal; and

A second phase detector circuit that connects the first clock circuit to the third clock circuit and is configured to generate the second error signal responsive to the first and the third clock signal and a second phase detector circuit. However, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to set a third clock circuit that is configured to generate a third clock signal responsive to a second error signal; and

A second phase detector circuit that connects the first clock circuit to the third clock circuit and is configured to generate the second error signal responsive to the first and the third clock signal. This is because Smith, III does disclose a second clock circuit configured to generate a second clock signal responsive to a first error signal and a first phase detector circuit that connects the first clock circuit to the second clock circuit and is configured to generate the error signal responsive to the first and the second clock signals. (See Figs. 1-2, col. 2, lines 65-67 to col. 3, lines 1-5 and lines 23-67 to col. 4, lines 1-60, and col. 12, claims 9-10).

As per claims 3-4, the teaching of Smith, III, has been discussed above, Smith, III further disclose a loop filter circuit (40) that is configured to generate a control signal at an output terminal thereof responsive to the first and second error signals;

An oscillator (28) that is configured to generate the first clock signal responsive to the control signal; and

A summation circuit (SUM 84). (See Fig. 6).

As per claim 6, this claim is rejected under similar rationale as set forth in claim 1.

As per claim 7, Smith, III further discloses wherein the first clock circuit, the second clock circuit, and the phase detector circuit are contained in a single integrated circuit chip. (See Fig. 1 and 2).

As per claims 8-10 and 12-13, these claims are rejected under similar rationale as set forth in claims 1-4 and 6-7.

As per claims 14-18, these method claims are rejected under similar rationale as set forth in the system claims 1-4 and 6.

As per claims 19-24, these claims are rejected under similar rationale as set forth in claims 1-4 and 6-7.

4. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, III (5,146,585) as applied to claims 1-4, 6-10 and 12-24 above, and further in view of O'Callaghan (3,518,472).

Claims 5 and 11, the teaching of Smith, III has been discussed above. Smith, III does not specifically disclose: A first amplifier circuit that is responsive to the composite error signal; and

A second amplifier circuit that is responsive to the composite error signal.

However, O'Callaghan discloses A first amplifier circuit (clutch amplifier 37) that is responsive to the composite error signal; and

A second amplifier circuit (brake amplifier 39) that is responsive to the composite error signal. (Col. 7, lines 29-34). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the first and second amplifier that are responsive to the composite error signal as taught by O'Callaghan into the filter of Smith, III in order to energize its winding when the instantaneous error voltage rises above or below a respective predetermined threshold.

5. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUNG My CHUNG whose telephone number is (571)272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Phung My Chung/
Primary Examiner
Art Unit 2117